

REMARKS

Claims 1 and 3-16 are pending in this application. By this Amendment, claims 1 and 3-16 are amended. The amendments introduce no new matter. Reconsideration of the application based on the above amendments and the following remarks is respectfully requested.

The Office Action rejects claims 1 and 3-16 under 35 U.S.C. §103(a) over U.S. Patent No. 5,349,366 to Yamazaki et al. (hereinafter "Yamazaki '366") in view of U.S. Patent No. 6,545,656 to Yamazaki (hereinafter "Yamazaki '656"). This rejection is respectfully traversed.

The Office Action concedes that Yamazaki '366 does not teach a horizontal scanning period that includes a first sub-horizontal scanning period to perform the setting step and a second sub-horizontal scanning period to perform the resetting step. The Office Action relies on Yamazaki '656 to remedy this shortfall. This combination of references fails for at least the following reasons.

First, the subframe periods, as shown in Figs. 2 and 3 of Yamazaki '656, can not reasonably be considered to correspond to a horizontal scanning period that includes a first sub-horizontal scanning period to perform the setting step and a second sub-horizontal scanning period to perform the resetting step as claimed. Specifically, the subframes of Yamazaki '656 do not perform the setting and resetting steps, as claimed. Yamazaki '656 teaches a reset signal R transmitted via the data line to the pixel TFT whereby the display of black is performed. In this way, the display of black is performed during one of the two subframes so that image persistence can be prevented (see col. 4, lines 32-51). As such, Yamazaki '656 does not teach, nor can it reasonably be considered to have suggested, a sub-horizontal scanning period to perform a resetting step that includes supplying a reset signal to select the non-conducting state of the driving transistor to the driving transistor via the data

line and the switching transistor in accordance with a period for which the second on-signal is supplied, as is recited, among other features, in the pending claims.

Second, the Office Action fails to establish a *prima facie* case for the combination of these references. The Office Action asserts that the motivation to combine the references is found: (1) in the fact that both teach similar matrix displays having set and reset functions within multiple frames; and (2) because set and reset functions are useful for providing a quality display as known in the art. Such broad conclusory statements do not point out specific objective evidence in the prior art that would have led one of ordinary skill in the art to combine these references in the manner suggested. Rather, these conclusions appear to be based on an application of impermissible hindsight reconstruction using Applicant's disclosure as a template to match claimed features.

The alleged set and reset functions disclosed in Yamazaki '656 are directed to preventing image persistence (see col. 2, lines 6-10). Yamazaki '366 is directed to providing a black and white display which is capable of rewriting only the desired pixels thereof, which stores the image at turning off the power, and restores it upon turning the power on again, which can sufficiently follow objects moving at a high speed, and providing a power-saving display capable of displaying gradation by a digital system. Significantly, Yamazaki '366 teaches a ferro-electric capacitor FE provided between the source of Tr_1 and the gate electrode Tr_2 , wherein the electric capacitor defines a lower limit for the potential V_1 (see col. 10, lines 24-29 and 57-61). Yamazaki '366 states that this arrangement is "distinctly different ... between the device according to the present invention and a conventional TFTLCD" (col. 10, lines 57-64).

A stated object of the subject matter of the pending claims is to provide a method for implementing the representation of the gray-scale of an electro-optical device without reset lines, according to the time ratio gray-scale method. Based on the structures and objectives of

the Yamazaki references, it would not have been obvious to one of ordinary skill in the art to combine the references in the manner suggested. In other words, it would not have been obvious to combine a reference intended to maintain image persistence through the use of a capacitor, with a reference that is intended to prevent image persistence. To do so would impermissibly alter the principle of operation of the primary references.

For at least the above reasons, the applied prior art references cannot reasonably be considered to have suggested the combinations of features positively recited in independent claims 1, 10-12, 15 and 16. Additionally, claims 2-9, 13 and 14 also would not have been suggested, by the applied prior art references for at least the respective dependence of these claims directly or indirectly on allowable independent claims 1 and 10, as well as for the separately patentable subject matter that each of these claims recite.

Accordingly, reconsideration and withdrawal of the rejection of claims 1 and 3-16 under 35 U.S.C. §103(a) as being unpatentable over a combination of the Yamazaki references are respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1 and 3-16 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

James E. Golladay, II
Registration No. 58,182

JAO:JEG/hms

Date: November 22, 2006

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

**DEPOSIT ACCOUNT USE
AUTHORIZATION**

Please grant any extension
necessary for entry;
Charge any fee due to our
Deposit Account No. 15-0461